24 Fall ECEN 704: VLSI Circuit Design

Design Pre-lab Report

Lab6: Differential Pairs

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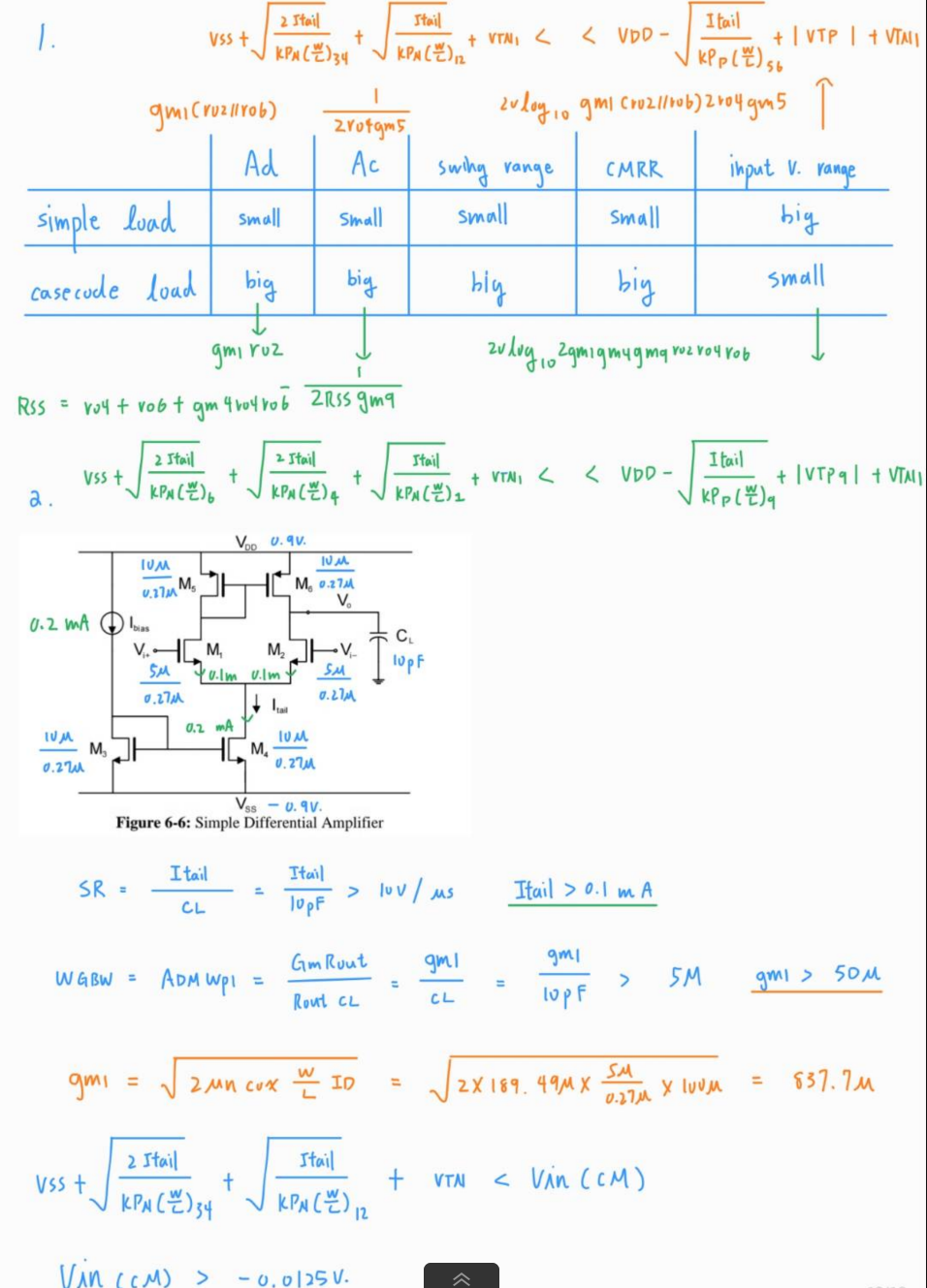
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1. Compare the two single-ended differential amplifiers discussed in this lab. Rate the differential gain, common-mode gain, output voltage swing range, CMRR and common-mode input voltage range. Include expressions for each design specification.
2. Design the simple differential amplifier in Figure 6-6 to obtain the following specifications:  
   Slew Rate > 10 V/μs  
   Gain-Bandwidth Product > 5 MHz  
   Common-mode Input Voltage Range > 0.5 V  
   Power Supply VDD = -VSS = 0.9 V  
   Load Capacitance 10 pF



1. Design the differential amplifier with cascode current mirrors in Figure 6-8 to obtain the following  
   specifications:  
   Slew Rate > 10 V/μs  
   Gain-Bandwidth Product > 5 MHz  
   CMRR > 60 dB  
   Power Supply VDD = -VSS = 0.9 V  
   Load Capacitance

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自動產生的描述